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During the reported SBIR phase I program, Microwave Monolithics Incorporated (MMInc.) investigated the feasibility of a new low temperature activation method for ion implanted GaAs processing. This approach taken by MMInc. is based upon the successful solid phase epitaxy developed for silicon integrated circuit processing. The work performed during phase I revealed a crystalline defect restriction to re-crystallation of the amorphous region. The major deterrent to the application of this approach in GaAs appears to occur during the complex amorphization step. Although this topic has high risk it has extremely high potential for improved processing technology needed for high frequency mm-wave devices.

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1.0) Introduction

Ion implantation is the only materials technology that permits
the high degree of control necessary for cost effective production
of advanced GaAs integrated circuits. Presently the only realistic
method of removing the ion implantation damages in III-V compounds
is by high temperature annealing. This high temperature method, is
restrictive to certain device profiles and fabrication techniques,
but even more serious it is detrimental to many advanced materials
such as HEMT and Ge/GaAs heterojunctions. These advanced structures
are severely damaged by the high temperature annealing methods and
many possible device and integrated circuits cannot be fabricated as
a result of these limitations.

In this program a new concept of annealing bombardment
damage is undertaken that has promise of performing removal of ion
bombardment damage at extraordinary low temperatures.
The achievement of conditions needed to accomplish this
amorphization/anneal method are complex and require detailed study
of the separate variables. Although the risk of this project is
high the benefits to SDIO are enormous. The application of this
technology to III-V integrated circuit processing would
revolutionize selective ion implantation for microwave, digital
and opto-electronic circuits. Mm-wave IC's which are bound to be
the most difficult to achieve would also benefit.

During phase I research on this low temperature activation of ion
implanted compound semiconductors Microwave Monolithics adopted an
approach that took advantage of prior work on GaAs and circumvented many
of the earlier difficulties shown to be a problem with solid phase
epitaxy in III-V semiconductors. The basic principles of this approach
are based upon the successful work of solid phase epitaxy in silicon
that has been developed to aid fabrication of advanced integrated
circuits. Our initial work has identified a problem in the complex
amorphization step that influences the successful application of this

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method. The solution to the problem of defect generation in GaAs amorphization will be resolved in future fundamental studies where greater attention can be spent with basic regrowth mechanisms as the potential of this powerful technique has yet to be exploited with III-V semiconductors.

2.0) Background Discussion

2.1) Basic Concepts

Low temperature activation or solid phase epitaxy has been studied in silicon and reduced to practice in recent years for use in controlling abrupt distributions of diffusion prone impurities. Amorphons layer generation in silicon and germanium is feasible due to a favorable strain-dose relationship as shown in Figure 2.1-1. As the amorphizing species (Si^+) is implanted into the Si lattice the crystal undergoes a linear strain relationship with increased dose all the way to a point where a coalescence of point defects occurs producing an amorphous crystalline state whose depth depends upon the energy of the bombarding species and the threshold for amorphization on the dose in ions cm^{-2}. Following amorphization a dopant species may be implanted within the amorphous region in the same manner as conventional ion implantation. Upon annealing the amorphized layer it has been demonstrated that recrystalization will occur at approximately one half the temperature for conventional implant damaged layers. Electrical activation of low temperature annealed Si layers ($550^{\circ}C$) is equivalent to that obtained at the more conventional ($1100^{\circ}C$) anneal temperature.

Substantial improvements have been obtained in control of doping distributions of rapid diffusing species using the pre-amorphized approach to ion implantation of Boron in Si.[1] Channeling, a common problem in the generation of abrupt profiles is also minimized by the use of a pre-amorphized substrate.
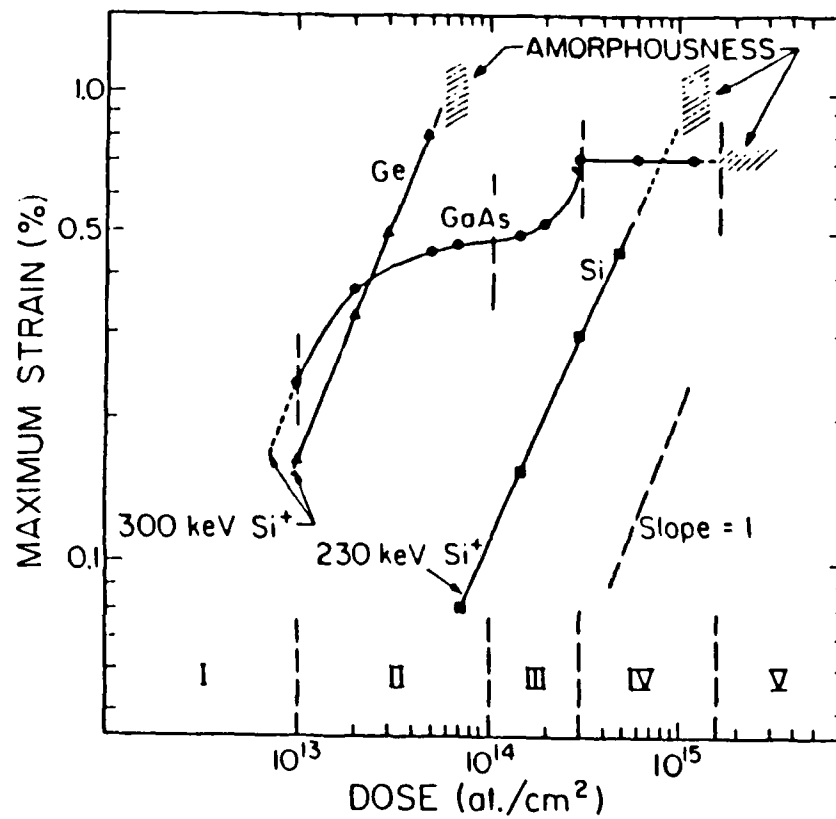
V.S. Speriousu et. al. Appl. Phy. Lett. 40, (7), (1982)

Figure 2.1-1) Maximum Strain as a Function of Dose

For GaAs, an amorphized low temperature regrowth method should greatly improve the processing of selective ion implantation for integrated circuit devices. At the present time a dielectric cap is used by most workers to offer surface protection and retard group V evaporation during the high temperature furnace anneal cycles. The diffusion of donor and especially acceptor impurities is very prominent in GaAs under the furnace anneal conditions. Impurities such as high dose Be, Mg and especially Zn experience high diffusion and broadening effects at high temperature making many device applications marginal to not feasible. Our interest in developing a low temperature activation technique for compound semiconductors has far reaching implications to making ion implantation feasible for temperature sensitive materials such as HEMT and multiple HEMT as well as strained layer materials that would not survive the normal post implant anneal cycle.

Other applications involve opto-electronic devices of ternary and quarternary III-V compounds grown and lattice matched to InP. The normal Zn and Cd acceptors diffuse very rapidly and have very limited annealing conditions for conventional ion implant processing.

2.2) Technical Approach

A similar general approach was taken for GaAs as was performed in silicon. The amorphizing implantation is done first at 77K and the dopant implantation is performed in situ with substrate temperatures held at 77K until all implants are complete. in this manner the heating effects from dopant bombardment are eliminated and no uncontrolled dynamic annealing should take place. For true epitaxy to take place, layer by layer, growth from the amorphous/crystalline interface should proceed upon heating to some critical temperature. In the section to follow a description of III-V amorphization, dopant implantation, and low temperature regrowth will be described along with characterization methods for measurement of thin crystalline layers near the surface. Electrical activity will also be addressed.

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2.3) III-V Amorphization

In GaAs the maximum strain as a function of dose is complex and occurs between 10^{13} and $10^{14} cm^{-2}$. The yielding effects of extended defects and stacking faults appear to be an irreversible transition occuring with room temperature amorphization. The intent of this program will be to perform an amorphizaton at 77K for purposes of eliminating generation of micronuclei that would later propagate during re-crystallization into faults and microtwins.

Defects propagating upon re-crystallization can lead to compensation of the doped region. It is clear from the work of Sadana et al[2] that doses in the range of $10^{15} cm^{-2}$ are required to produce full amorphization in GaAs. It is not clear whether displacement effects will occur to interfere with an ordered layer by layer regrowth performed at low temperature. If As^{+} is a bombarding species there is also possibility of precipitation effects in the lattice to produce nucleation centers for defects growth upon recrystallation. The compound region in the GaAs phase diagram becomes quite narrow at lower temperatures and solubility restraints could be a problem where self diffusion is also limited. The case for elemental semiconductors is most ideal where displacement effects are not detrimental and only solubility limits the extent of doping in the pre-amorphized region.[3]

2.4) Dopant Implantation

Introduction of a dopant species in GaAs may be performed following amorphization in situ at 77K, or before amorphization. The important self annealing problem should be avoided by holding the substrate always at 77K. Knock-on distributions have not proven to be a difficulty in GaAs for post-amorphization approaches. The desired dopant species for this work is $^{29}Si^{+}$. The pre-amorphization damage could be broken up by a post-amorphization which could provide the final assurance for full amorphization. In any case the entire amorphization stage carries

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limited information until annealing is achieved and then the data contains several variables.

The introduction of dopant into a pre-amorphized region has been pursued in GaAs as was performed in Si and Ge. The major difficulty in the dopant implant is the dynamic annealing effects that occur with room temperature implants. Later regrowth of the partially re-crystallized region leads to propagation of defects that produce compensating effects upon the activation of implanted carriers. For amorphization in silicon control of substrate temperature resolved the problem of dynamic annealing and low carrier activation. In GaAs problems related to dynamic annealing are present for all room temperature implants. In addition the low temperature amorphized layers in GaAs all tend to regrow with major defects. Re-crystallation of low temperature amorphized GaAs proceeds at low temperature, but not without propagation of stacking faults and extended defects.[2] Before the dopant implants can be activated the problem of severe defect generation needs to be resolved.

2.5) Low Temperature Regrowth

Si amorphous layers regrow on a hypothetical layer by layer basis and leave little trace of defect regions. The exception of course is solubiity limitations and non-ideal a/c interfaces. Small clusters (>15Å) of point defects can propage to form small embryonic dislocation loops. Interstitial Si atoms can also coalesce to form loops.[3] In GaAs several other problems are possible:

1) Displacement effects
2) Stoichiometry related effects
3) Solubility limit effects
4) Interstitial problems
5) Ordering effects
6) Thermal activation threshold

Displacement effects from bombardment of a layered III-V
semiconductor could result in long range disorder making crystalline
reconstruction difficult and prone to effects of interstitial and
antisite defect generation. The effects of displacement are very
difficult to assess as the amorphized layer is not prone to
characterization methods that will yield analytical data. Post regrowth
analysis revealing interstitial and antisite defects need to be
corollated with other factors such as stoichiometry and solubility.

Stoichiometry effects from atomic displacement could produce
compensation or other dopant activation anomalies. Also precipitation
of As would invoke a stoichiometry imbalance if excess As could not
escape during the re-crystallation step.

Solubility limit problems in GaAs are normally not experienced due
to the requirements for doping in existing device structures. As^+
bombardment could exceed solubility limits for the compound and as such
could contribute to stoichiometry, antisite defects or precipitation
problems leading to crystalline regrowth defects.

Interstitial effects can be produced by solubility limit
difficulties as in the case of high As^+ doses that remain in the lattice
following annealing. Ordering effects experienced with lattice defects
disturbing the A-B structure in GaAs can also produce interstitial
defects of excess Ga or As.

Ordering effects as mentioned earlier can be the result of lattice
defects (point defects or extended defects) due to the disruption of
continuous growth. Interstitial atoms (As^+) could also induce ordering
effects by straining the lattice. Precipation due to As^+ clustering and
solubility limit problems can also incite non-continuous crystal growth.

Thermal Activation threshold requirements are expected to be
different to crystalline regrowth conditions. The lattice mobility
necessary for high dopant activity has been demonstrated in non-

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amorphized GaAs to be achieved at a higher temperature than that for recrystallation.

2.6) Characterization of Amorphized Layers

Measurement of amorphized layers can be accomplished before re-crystallation to document amorphized depth and lack of crystallinity. Re-measurement following regrowth can be referrenced to show remanent damage effects. The following techniques have been used successfully to characterize both Si and GaAs amorphous layers.

Diffraction Techniques:

1) HRTEM: Images crystalline order and gives excellent distinction of relative crystalline perfection

2) SEM: Angular diffracted patterns can produce a qualitative indication of crystallinity on a low sensitivity scale.

Scattering Techniques:

1) RBS: Rutherford back scattered protons or He^+ ions are used to measure thick layers penetrated by MeV accelerated ions. A well disordered layer will show major differences between one that has good crystal perfection. No arguments about crystal quality can be made, only relative comparisons.

2) Ellipsometry: The extinction coefficient is extremely sensitive to damage effects and is useful as a profiling method when used in conjunction with a thinning etch. Figure 2.6-1 shows a damage profile produced with Si^+, 320KeV, $6E12cm^{-2}$ before and
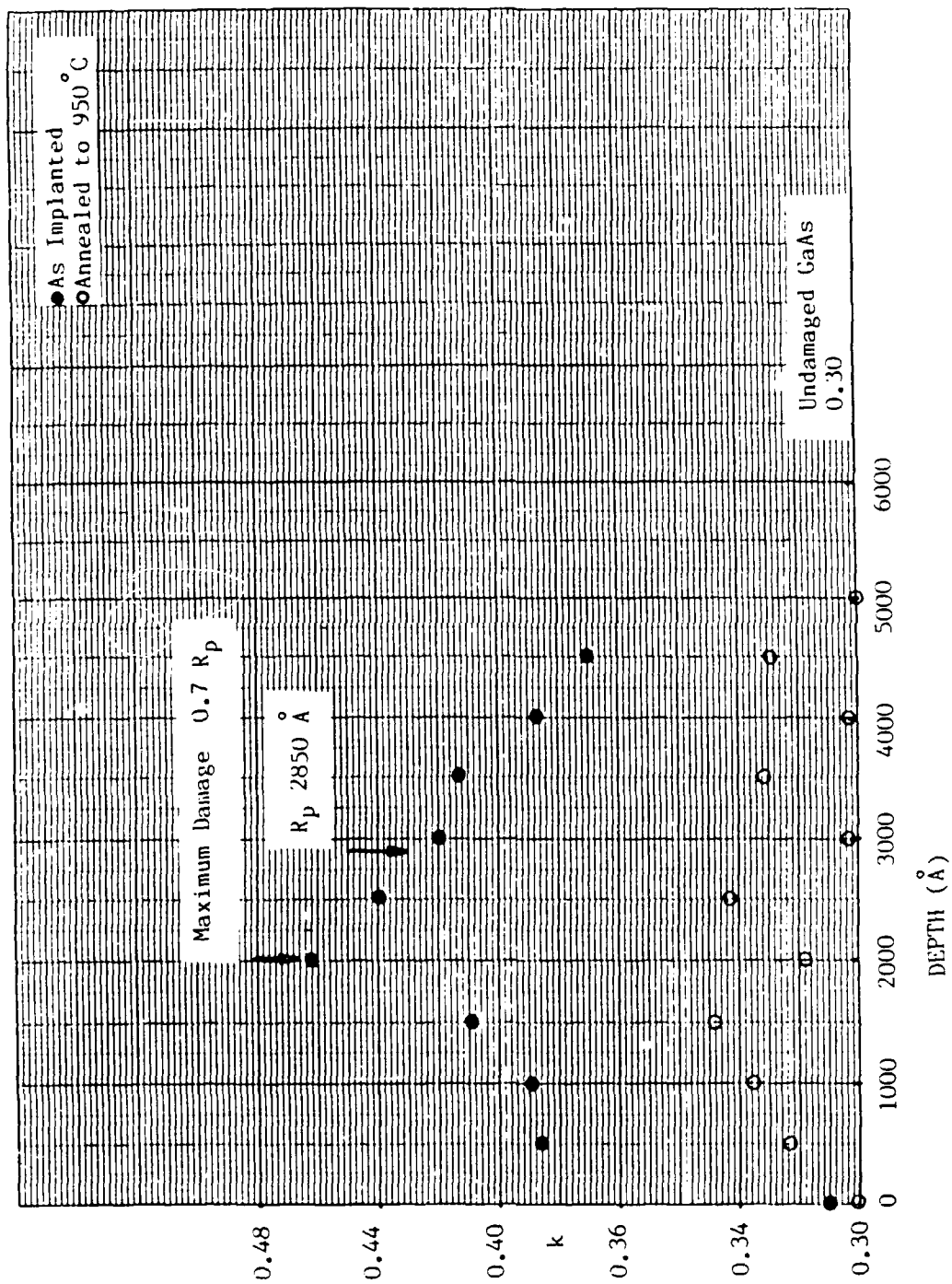
8

Figure 2.6-1) Damage Depth Profile by Ellipsometry

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after annealing. Even following re-
crystallization that produced >80%
electrical activation the residual damage
level is discernible.

3) IR Reflectance: Infrared reflectance techniques
can also be used to detect amorphous layer
depth using optical interference methods.

4) Differential   Etch delineated bevel or groove
   Etch Methods: measurements can be made with a
                    profilameter.

5) Optical   Visable reflectance shows a
   Refelctivity: contrast change in the surface
                    reflectance of damaged GaAs. An
                    "as implanted" GaAs surface
                    appears lighter than as polished
                    surface. Heavily bombarded GaAs
                    surfaces (500KeV, $1E15cm^{-2}$)
                    look light yellow in appearance.
                    The regrown or annealed surfaces
                    return to original appearance of
                    a polished wafer.

2.7) Electrical Activity

Electrical measurement of dopant activity in regrown GaAs layers
can be performed with the customary tools for thin layer measurement.
Electrical assessment using resistivity and Hall measurement are
performed. The measured distribution of dopants by profiling is
essential to show the corollation with LSS projections. Trap
measurements can be used to identify deep damage centers effecting full
carrier activation. Additional corollation with chemical distributions

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can be obtained with Secondary Ion Mass Spectrometry (SIMS) for Si
implanted layers, where projected depth is >1000$\overset{\circ}{A}$.

3.0) Phase I Research and Results

  3.1) Modified Approach

In order to obtain an amorphised layer deep enough for typical
"device" dopant implants an energy in excess of 400KeV is required.
Our earlier approach using commercial 200KeV ion implantation
equipment and doubly charged As would give only a 1500$\overset{\circ}{A}$ separation
between the 120KeV Si$^+$ implant and the amorphous-crystalline interface.
In order to place a greater margin of safety a revised approach was
taken where a higher energy source could be used. A research
accelerator with MeV capability for inert ions was available through
California State University - Los Angeles. In this apparatus Ar$^+$ was
used to provide both 500KeV and 1MeV at 1E15cm^{-2} fluences. The
calculated damage depth for Ar$^+$ at these accelarations are as follows:

$$500\text{KeV Ar}^+: \quad \underline{2400\overset{\circ}{A}}$$
$$1\text{MeV Ar}^+: \quad \underline{4200\overset{\circ}{A}}$$

The bombardment damage should extend in from the surface and not
require a multiple energy approach as suggested earlier. The calculated
amorphized envelope is shown with the projection for the Si$^+$ dopant
implant in Figure 3.1-1 and 3.1-2. In order to assure the validity of
the dopant implant it was performed first and portions of that sample
evaluated by conventional means before the amorphization was performed.
In this manner the critical amorphization step was last and would
possibly have less complications from dynamic annealing. In the
sections to follow a description of the full experimental procedure and
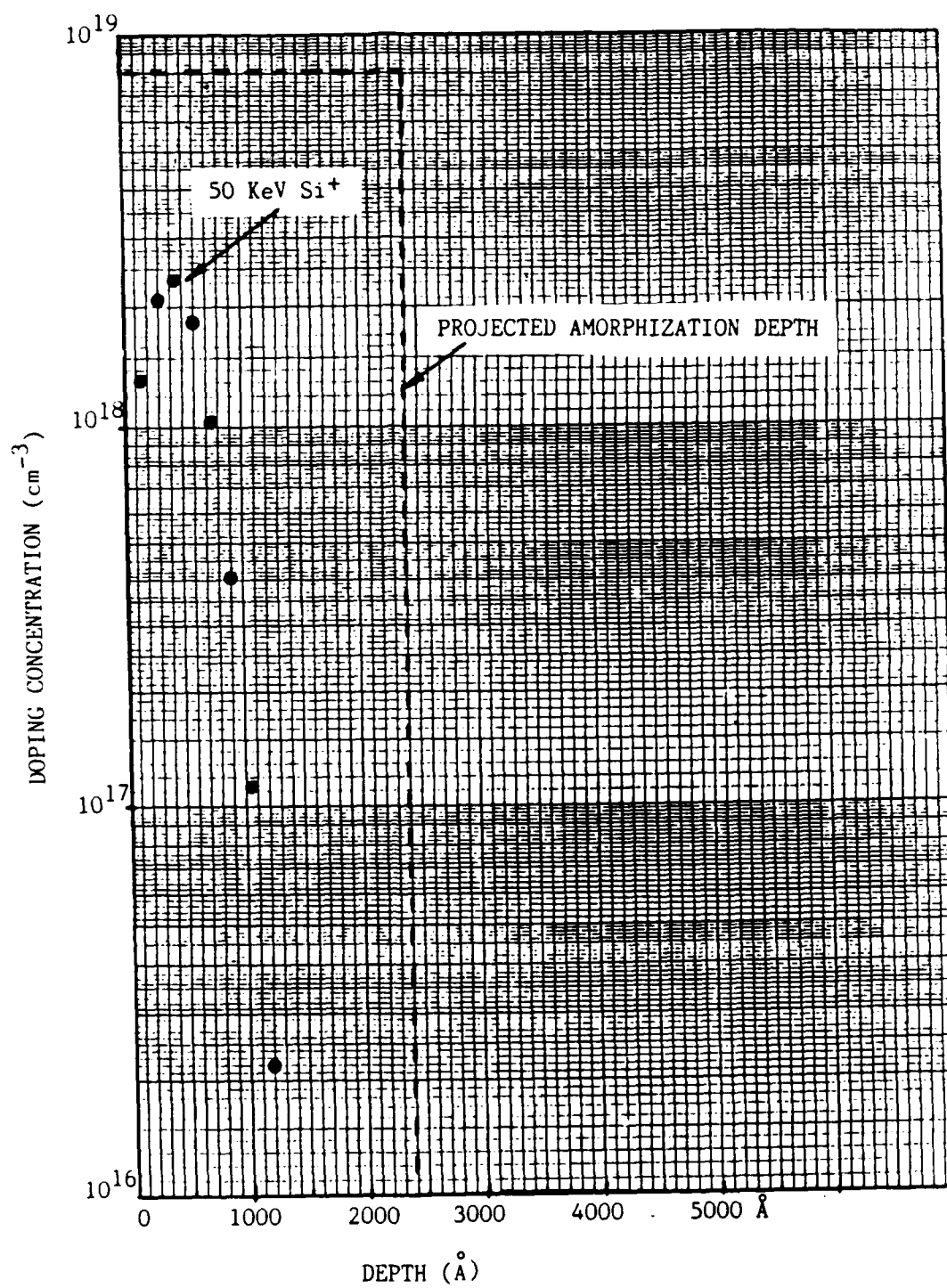results will be shown.

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Figure 3.1-1) Projected Amorphization Profile with 50KeV Si$^+$ Distribution
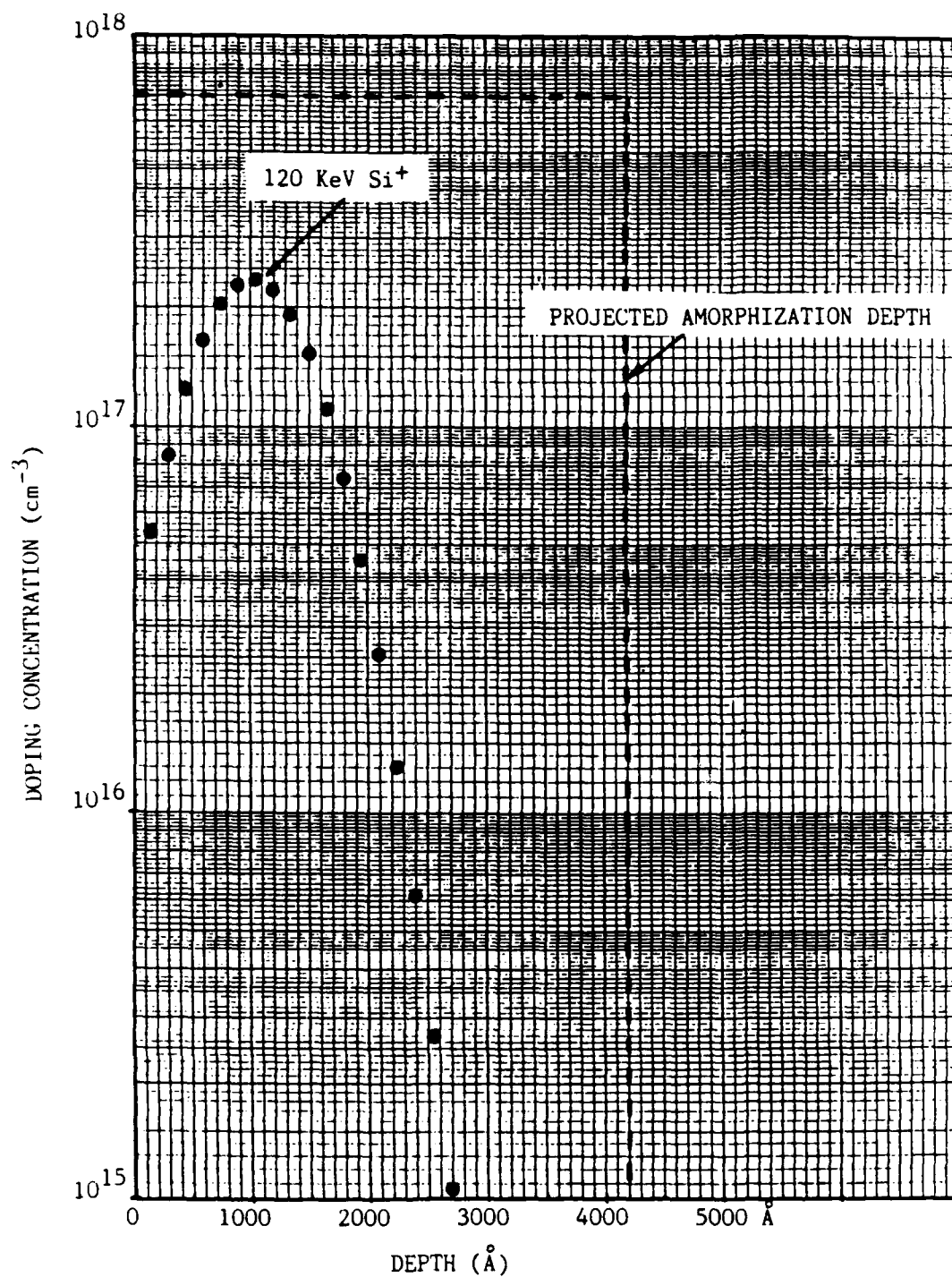
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Figure 3.1-2)   Projected Amorphization Profile with 120KeV Si⁺
                Distribution

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3.2) Experimental Procedures - Wafer Preparation

High quality semi insulating GaAs substrates were selected for this
study that had the following properties:

Resistivity: $>10^7 \Omega$-cm

Mobility: >5000 cm^2/v-sec

Thermal Stability: $>10^7 \Omega/\square$ following anneal to 950°C

Ion Implantation: $>80\%$ carrier activation with
^{29}Si$^+$ and 950°C anneal conditions

3.3) ^{29}Si$^+$ Ion Implantation

Two separate ^{29}Si$^+$ implants were used in this study to evaluate the
low temperature amorphization and low temperature regrowth as follows.

1) 50KeV, 1.5E13cm^{-2}

2) 120 KeV. 3.0E12cm^{-2}

The above implants were performed by implanting ^{29}Si$^+$ produced from
an ionized beam of SiF$_4$. The implants were made at room temperature
with beam currents of approximately 10uA. To verify the Si$^+$ implants a
small piece was annealed before amorphization by the flash anneal method
and the resulting carrier profile evaluated by the C-V method. The
carrier profiles from the activated 50KeV and 120KeV implants are shown
in Figure 3.4-1.

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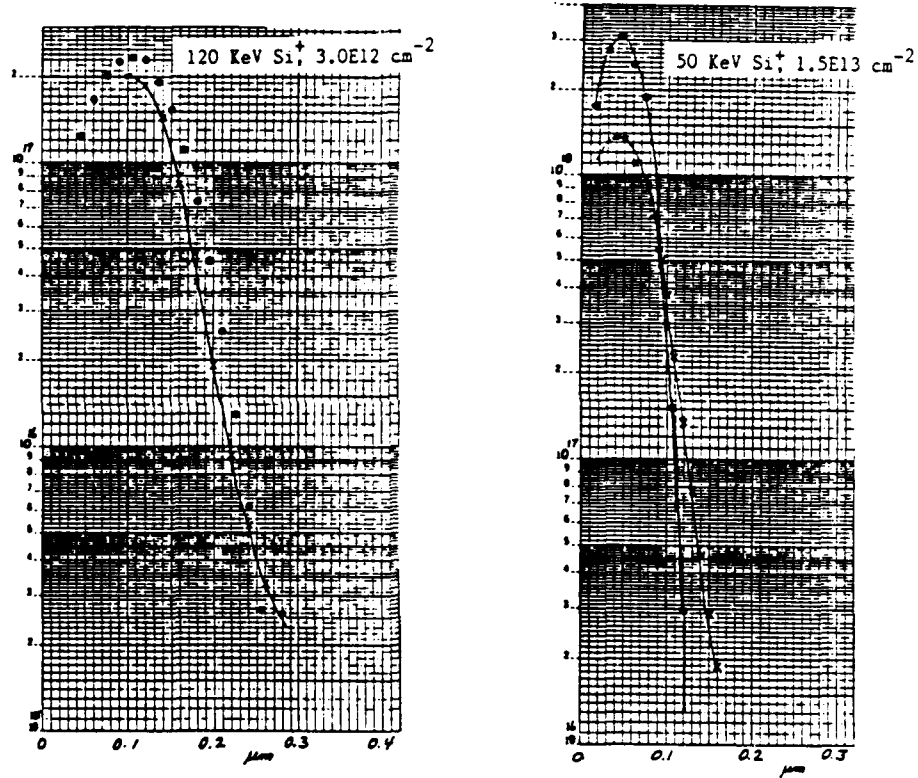CONVENTIONAL HIGH TEMPERATURE POST ION IMPLANT ANNEAL OF Si$^+$

Figure 3.4-1) Activated ^{29}Si$^+$ Profiles for 50KeV and 120KeV Implants

The carrier profiles are shown with LSS projections to show the corollation between the observed and theoretical distributions for $^{29}Si^+$. The profiles are both of good activation and show abrupt profile corollation with the LSS data. The remaining protions of these $^{29}Si^+$ implanted slices were taken for low temperature amorphization bombardment with Ar^+.

3.4) Low Temperature Amorphization

Samples implanted with 50KeV $^{29}Si^+$ and 120KeV $^{29}Si^+$ were mounted on a specially constructed heat sink for reduced temperature bombardment. A diagram of the holder is shown in Figure 3.5-1. The interior of the substrate holder was machined to allow a liquid N_2 cooling channel for efficient transfer of heat from the GaAs undergoing bombardment. Small Be-Cu clips hold the GaAs securely against the cooled holder. The assembly is inclined 7° to the beam to reduce effects of channeling. For bombardment the sample holder is mounted in the end station of a High Voltage Engineering Accelerator and evacuated prior to bombardment. Sample cooling is initiated by flowing LN$_2$ thru the sample holder held under vacuum. When the sample holder passes liquid N_2 the bombardment is started using an ionized Ar^+ beam. The beam is magnetically raster scanned across the target area. A precision dose integrator is used to collect the charge from the sample. The cooling is maintained during the bombardment period and the beam is terminated by the dose integrator when the desired charge is achieved. Following bombardment the cooling is terminated and the sample is slowly warmed to room temperature by ambient temperature. The sample is removed and replaced with another pre-implanted slice and the cycle is resumed.
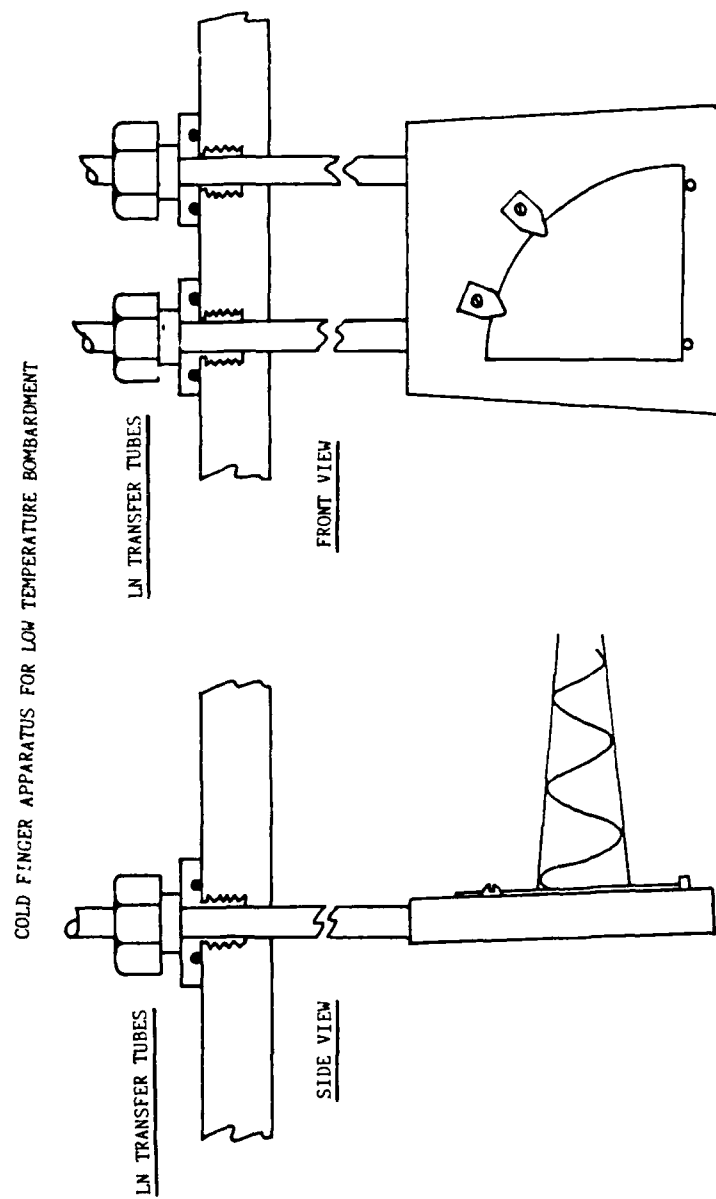
COLD FINGER APPARATUS FOR LOW TEMPERATURE BOMBARDMENT

LN TRANSFER TUBES

FRONT VIEW

LN TRANSFER TUBES

SIDE VIEW

Figure 3.5-1) Sample Holder for Low Temperature Bombardment

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The schedules for Ar$^+$ amorphization are as follows:

Sample	Si$^+$Implant	Ar$^+$Amorphization	Temperature
2075-020	50KeV, 1.5E13cm^{-2}	1MeV, 1E15cm^{-2}	77K
2075-012	120KeV, 3.0E12cm^{-2}	500KeV, 1E15cm^{-2}	77K

3.5) Low Temperature Annealing

Amorphized samples of both the 50KeV Si$^+$ implant and the 120KeV Si$^+$ implant were annealed at temperatures between 400-950°C as follows:

1) 400°C: Low temperature annealing was performed in reducing atmosphere (Forming Gas) in a face down configuration as shown in Figure 3.5-2. The apparatus as shown utilized a petri dish and a domed cover to introduce the protective atmosphere. A hot plate was used for heating the assembly to temperature. In operation the hot plate was heated to temperature and the pre-purged assembly with wafer was transferred for rapid heating to 400°C. Following a 20 minute anneal the assembly was moved off the hot plate and allowed to cool before the sample was removed.

2) 500°C: Intermediate temperature annealing was performed in a reducing atmosphere (forming gas) using a flash anneal apparatus as shown in Figure 3.5-3. The heat source in Figure 3.5-3 was a 9 KW bank of quartz halogen lamps controlled by an SCR power supply. The saample was placed face down and purged with forming gas for 15 minutes prior to heating. The control temperature was reached in 2 minutes by slowly ramping the lamp power to the indicated 500°C displayed by a chromel-alumel thermocouple positioned near the sample. Following a 20 minute anneal the lamps were turned gradually off and the apparatus cooled to room temperature before removing the sample.

3) 600°C: The highest gradual anneal was performed at 600°C in the flash anneal apparatus described in 2) as shown in Figure 3.5-3. The

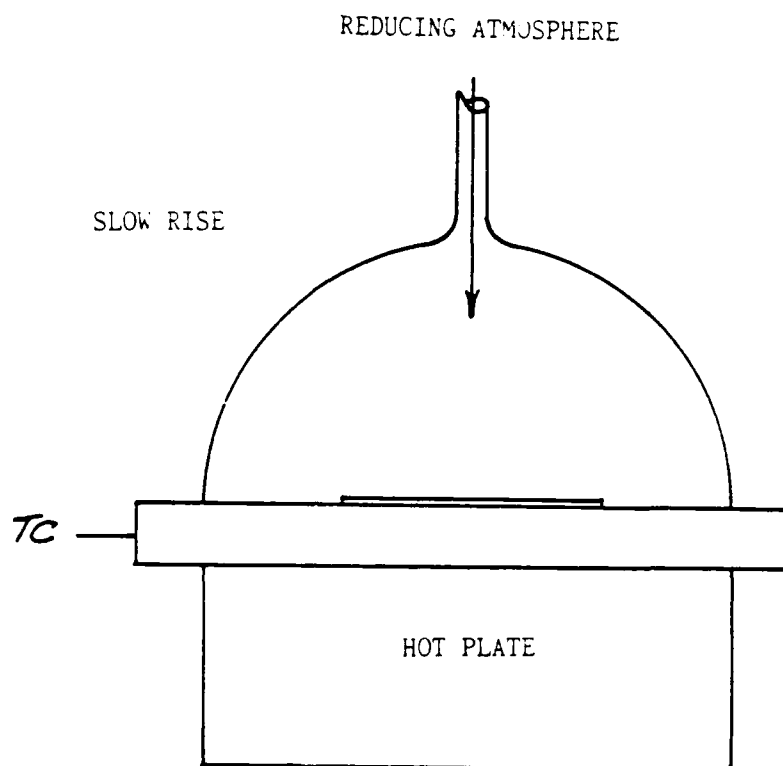REDUCING ATMOSPHERE

SLOW RISE

TC

HOT PLATE

Figure 3.5-2) Hot Plate Anneal Apparatus

heating was performed in the same manner as in 2) only heating to 600°C for 15 minutes before cooling to ambient temperature.

4) $\underline{950^{\circ}C:}$ Samples failing to activate at the lower temperatures were heated in the flash anneal apparatus to 950°C as a conventional room temperature implant would be processed. This mode of annealing was used to activate the Si^{+} implants shown in Figure 3.5-3 for purposes of verifying the implants prior to Ar^{+} bombardment.

The samples taken from annealing 1-4 were inspected by optical microscopy and taken to a C-V apparatus and contacted with a Hg probe for rapid measurement of electrical activation.

Table 3.5-1 shows a summary of the data produced in low temperature annealing experiments.

Table 3.5-1

<u>Low Temperature Annealing of Amorphized GaAs</u>

<u>Sample</u>	<u>Anneal Temperature</u>	<u>Anneal Period</u>	<u>Observations</u>
2075-012	400°C	20 minutes	Yellow
2075-012	500°C	20 minutes	Yellow
2075-012	600°C	15 minutes	Grey
2075-012	950°C	8 seconds	Grey

SCHEMATIC DIAGRAM OF FLASH ANNEAL FURNACE

AIR COOLING

REFLECTOR

QUARTZ HALOGEN LAMPS

GaAs SUBSTRATES

THERMOCOUPLE

SILICON SUSCEPTOR

VENT

FORMING GAS AMBIENT
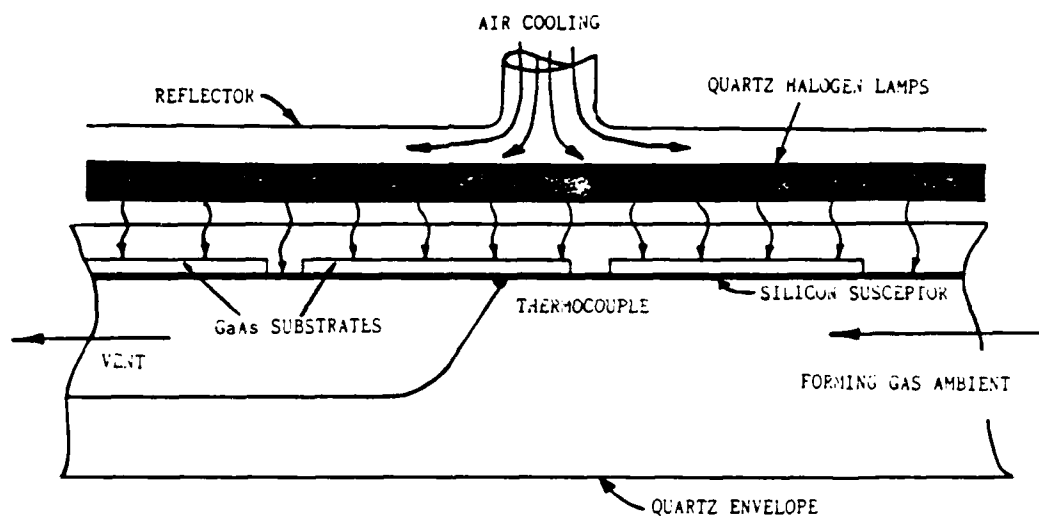
QUARTZ ENVELOPE

Figure 3.5-3) Flash Anneal Apparatus

3.6) Characterization of Low Temperature Regrowth - Electrical Measurements

Following low temperature anneal the Si^+ implanted-amorphized layers were measured on a C-V apparatus as used for Figure 3.4-1. The C-V measurement system used was a Material Development Corporation Analog profiler. To profile a layer the bias voltage is set to near breakdown voltage of the Hg Schottky barrier under reverse bias (-). The analog system ramps the bias to zero and a log-log plot of N(x) vs x is obtained. The system can also be operated manually at any bias point for point data as well. The verification data on the 50KeV and 120KeV Si^+ implants in Figure 3.4-1 was obtained using the above apparatus.

Data taken from annealed samples following low temperature regrowth are shown in Table 3.6-1.

Table 3.6-1

Capacitance Measurements of Low Temperature Regrown Layers

Sample	Si^+ Implant	Ar^+ Bombardment	Anneal Temperature	$C_{(o)} pF/cm^2$
2075-012	120KeV, $3E12cm^{-2}$	500KeV, $1E15cm^{-2}$	$600^{\circ}C$, $950^{\circ}C$	<0.1pF
2075-020	50KeV, $1.5E13cm^{-2}$	1MeV, $1E15cm^{-2}$	$600^{\circ}C$, $950^{\circ}C$	<0.1pF

Further measurement of samples not indicating a capacitance were made by using Indium contacts in a Van der Pauw configuration. The samples were approximately 7mm on a side and were biased to 25v, far from any critical breakdown fields. The sheet resistance data from these samples is shown in table 3.6-2.

Table 3.6-2

Sheet Resistance of Low Temperature Regrown Layers

Sample	Si$^+$Implant	Ar$^+$Bombardment	Anneal Temperature	Sheet Resistance
2075-030	-0-	-0-	950°C	6.2E9 Ω/□
2075-020	50KeV, 1.5E13cm^{-2}	1MeV, 1E15cm^{-2}	600°C, 950°C	1.9E8 Ω/□
2075-012	120KeV, 3E12cm^{-2}	500KeV, 1E15cm^{-2}	600°C, 950°C	4.7E7 Ω/□

3.7) Characterization of Amorphized Layers – Crystalline/Amorphous Measurements

Following bombardment of the Si$^+$ implanted samples the layers were measured by ellipsometry to determine amorphous layer depth. The extinction coefficient as described in 2.6 is sensitive to lattice damage and disorder.[4] Samples of amorphized GaAs were measured before and after annealing with a Rudolph Model EL-III ellipsometer. The 6328Å He-Ne laser line was used for sampling the optical properties of the near surface region. In order to obtain profiles the samples were etched in 500Å steps and remeasured at each step until the interface was reached. Figure 3.7-1 shows a 50KeV Si$^+$ implant with 1MeV amorphization before and after annealing to 600°C. The fact that the annealed values are only one-half the magnitude of the damaged ones is indicative of the remanent damage remaining in the layer following anneal.

Assessment of crystal quality following low temperature regrowth was made by electron diffraction and RBS measurement.

Electron Diffraction: Samples implanted and bombarded with Ar$^+$ were measured by imaging the angular reflected electrons from the top 2000Å nearest the surface with a 20KV electron beam. Samples were

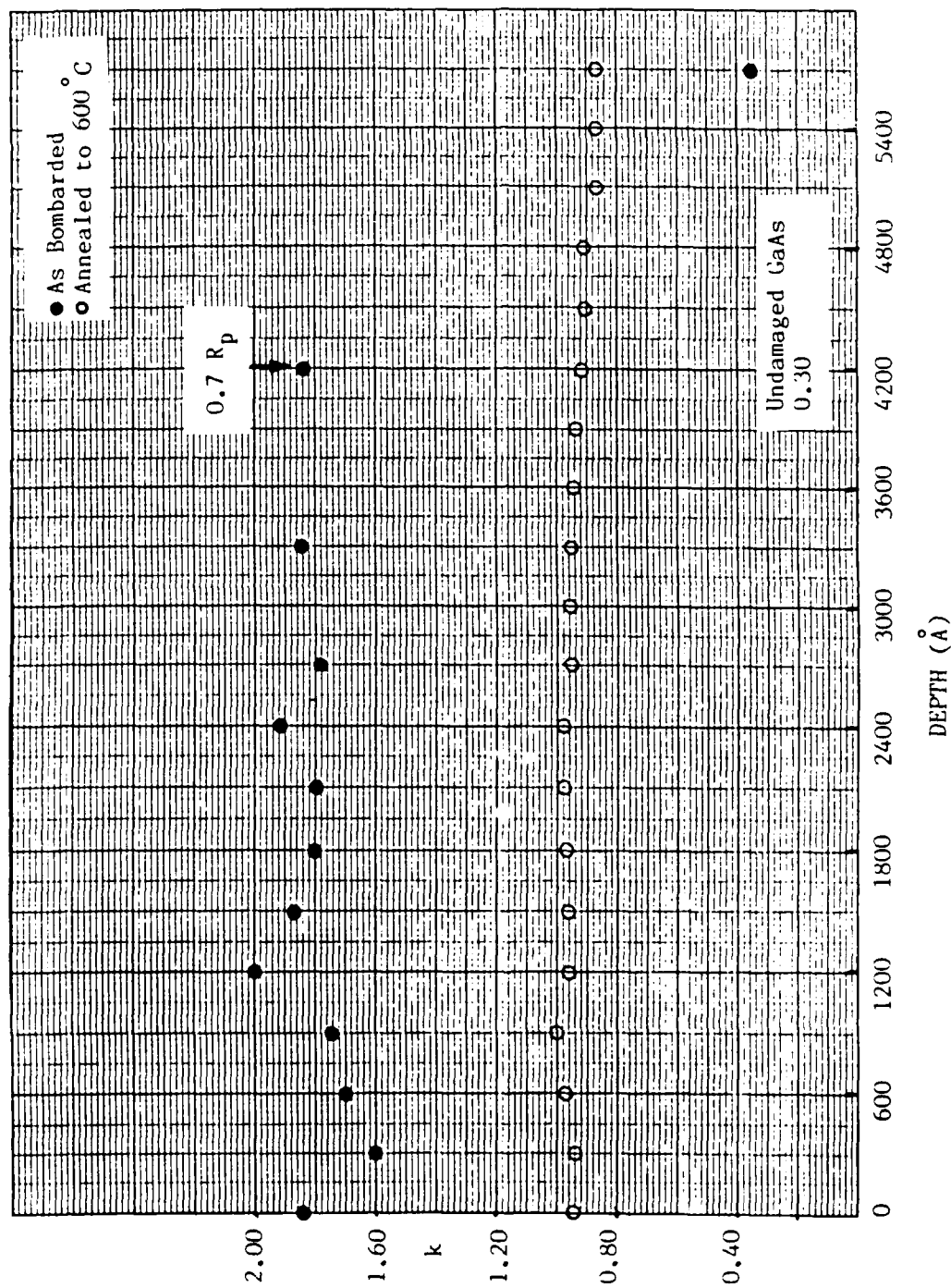50 KeV Si$^+$, 1.5E13 cm^{-2}, 1 MeV, 1E15 cm^{-2} Ar$^+$

Figure 3.7-1) Damage Depth Profile for 50KeV Si$^+$/1MeV Ar$^+$

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selected from the 50KeV and 120KeV implant that were measured as bombarded, and after annealing to 600°C. For reference purposes a sample of undamaged GaAs from the same ingot was included for comparison. Figure 3.7-2 shows the undamaged (a), as damaged (b) and annealed (c) for the 120KeV, 3.0E12cm^{-2} with 500KeV Ar^{+} bombardment. Figure 3.7-3 shows a similar set for the 50KeV, 1.5E13cm^{-2} with 1MeV Ar^{+} bombardment. The reflected electron diffraction figures in 3.7-2 and 3.7-3 show reasonable diffracted images for the undamaged substrates, but no evidence of reconstruction for either the 50KeV or 120KeV implant. The extent of bombardment damage on the 500KeV and 1MeV samples show no discernable differences between as bombarded and annealed for annealing to 600°C for 10 minutes.

Rutherford Back Scattering (RBS): Samples were bombarded with 4MeV He^{+} ions and backscattered He ions were measured at 55° for samples "as bombarded" with Ar^{+} and those after annealing at 600°C. Figure 3.7-4 shows a RBS plot of count vs channel number for the 120KeV Si^{+} implant bombarded with 500KeV Ar^{+} at 1E15cm^{-3}. Figure 3.7-5 shows the RBS measurement for 50KeV Si^{+} bombarded with 1MeV Ar^{+} at 1E15cm^{-2}. The before and after annealing measurement of the 500KeV Ar^{+} bombardment in Figure 3.7-3 shows some signs of damage removal after the 600°C anneal. In Figure 3.7-5 the before and after anneal data, for the 1MeV bombardment indicating minimal damage removal.
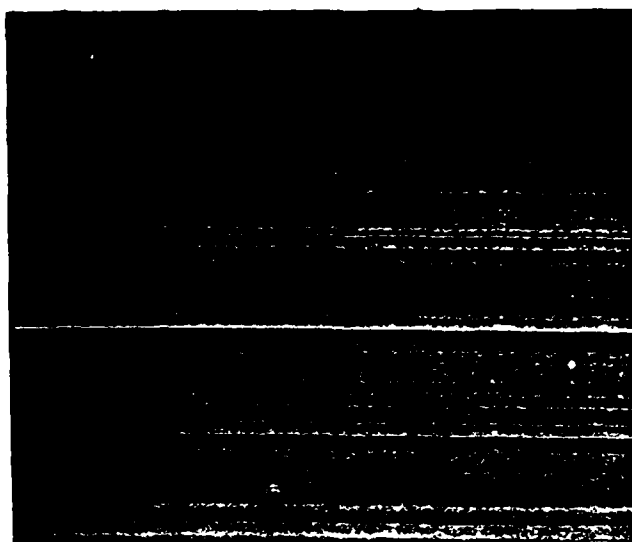
4.0) Summary and Recommendation

Bombardment of GaAs with high energy Ar^{+} ions produced a deep amorphized region in excess of the 50KeV and 120KeV Si^{+} ion implants in the samples studied. However attempts to regrow the amorphous region by low temperature annealing were ineffective. The electrical activation of Si^{+} implants in the Ar^{+} bombarded samples was obscured by the compensating effects of residual crystalline damage. The program phase I results can be summarized as shown below:
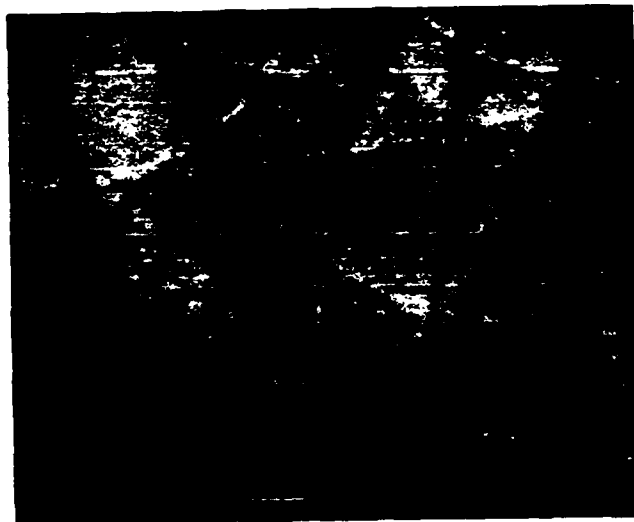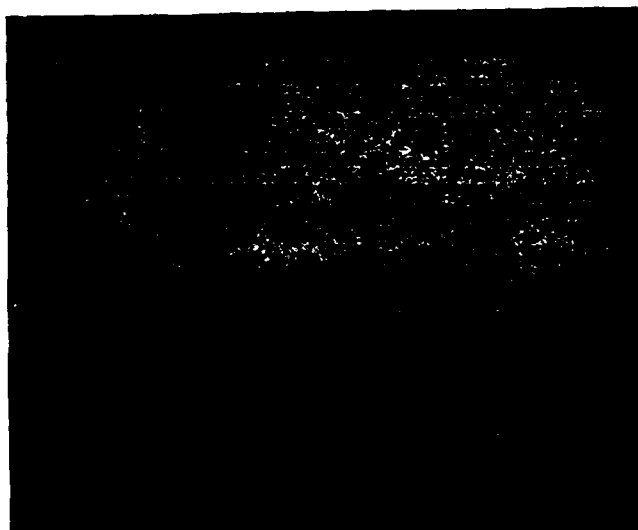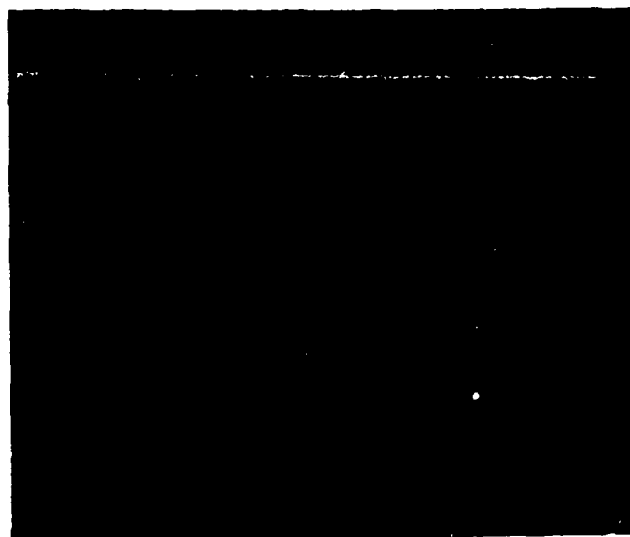
25
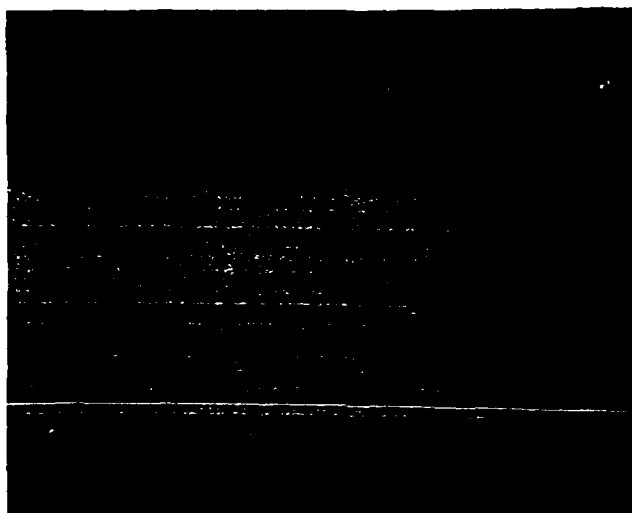
UNDAMAGED

AS BOMBARDED

ANNEALED TO 600°C

Figure 3.7-2) Electron Diffraction of Regrown 500KeV Ar$^+$ Samples

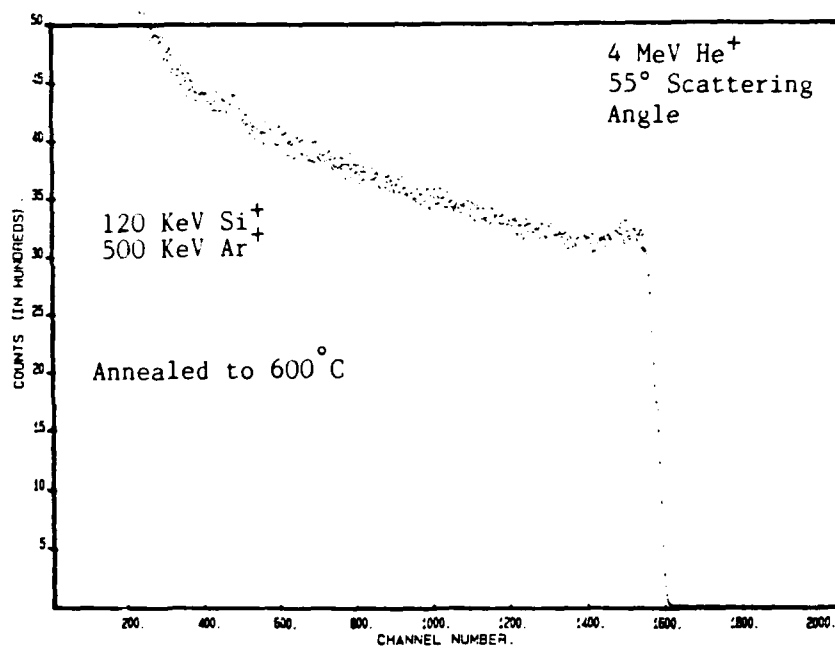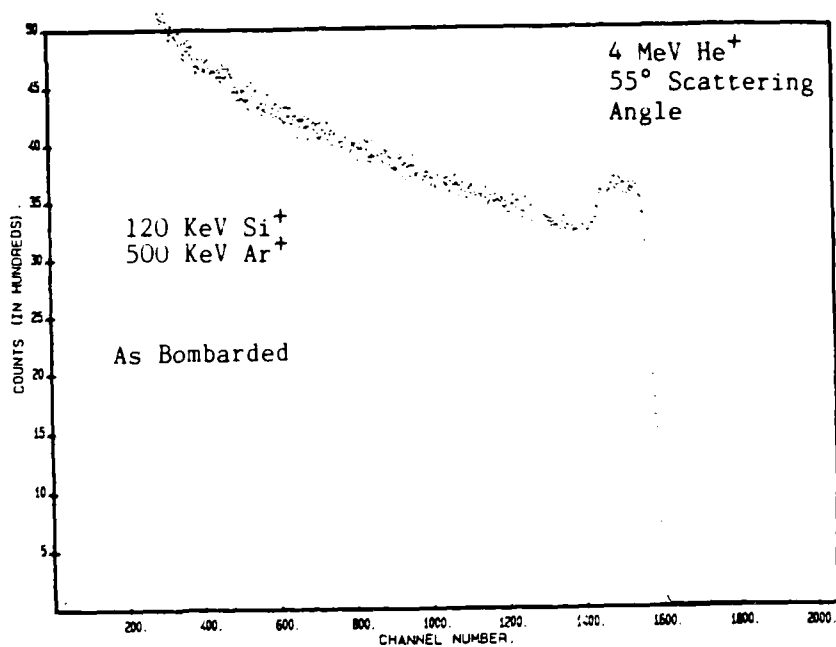Figure 3.7-3)   Electron Diffraction of Regrown 1MeV Ar$^+$ Samples

Figure 3.7-4)   Rutherford Backscattering Profile - 500KeV Ar⁺

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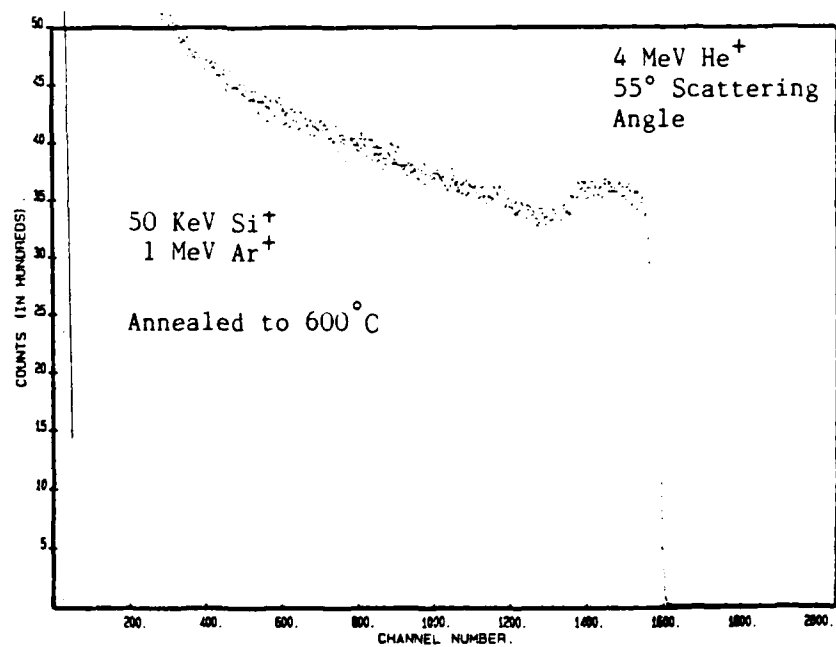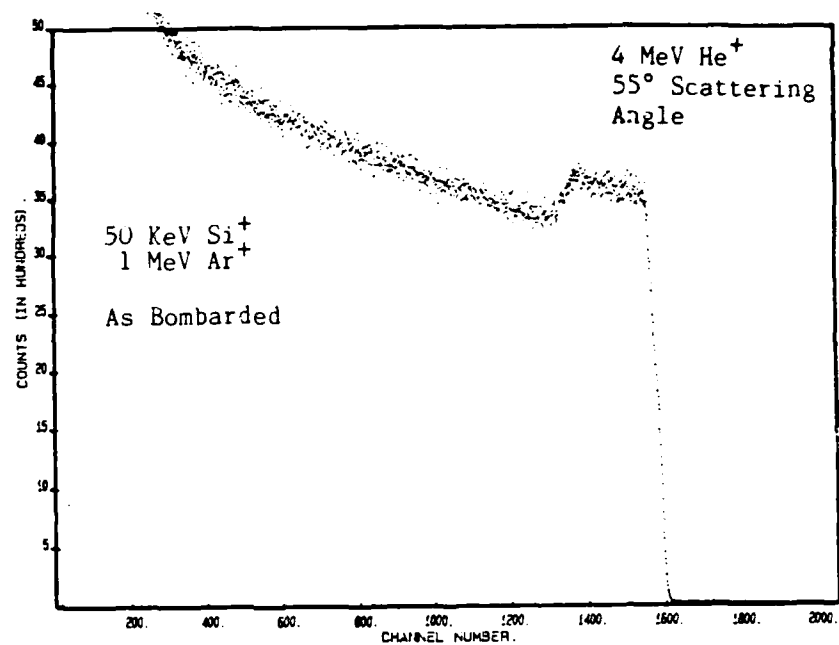Figure 3.7-5) Rutherford Backscattering Profile - 1MeV Ar$^+$

Tasks Performed	Evaluation Method	Results
Amorphization of GaAs with 500KeV, 1MeV Ar^+	Ellipsometry	Deep damage >4000Å
Pre-implant $^{29}Si^+$ 50KeV, 120KeV	Flash annealed, C-V profile data LSS projection for Si^+	Carrier profiles in agreement with LSS projections
Low temperature annealing to 600°C in reducing atmosphere	Ellipsometry, C-V, resistivity meas. RBS, electron diffraction	Incomplete re-cryatallation
Assessment of low temperature activation of Si^+	C-V, Resistivity measurement	No apparent activation of Si^+ due to residual bombardment damage

A focus of the major difficulty experienced in phase I was the problem producing high quality regrown layers. The extent of damage in the Ar^+ bombardment appeared to be in excess of what could be removed by annealing. Anneal temperatures up to 950°C were not effective in regrowing the damaged region. We believe the major difficulty resides in the method of producing the amorphous layer and not the annealing method providing a sufficiently high temperature.

We therefore recommend that future research be focused primarily upon the basic amorphization step and use impurity implants only as a demonstration of electrical activity in high quality regrown layers. In our study the 77K variable was not the only factor in preventing a source of defects from forming that would later complicate low temperature epitaxy. We believe 77K bombardments will circumvent the generation of point defects and extended defects from dynamic annealing, but crystalline regrowth problems can also arise from the following effects:

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Primary Effect	Result
1) Displacement Effects	Long range disorder of compound semiconductor lattice, anti site defects, interstitials, precipatates
2) Solubility Limit Effects (As^+)	Anti site defects, stoichiometry defects, interstitials and precipitates
3) Inert Gas Solubility Effects	Interstitials leading to deep electrical defects with compensating effects on shallow impurities

Resolution of the above three effects will require definitive HRTEM measurements in a study of amorphizing _species_ and _dose_ for energies >500KeV.

A recommendation of As^+ as the desired amorphizing species is also important.

Unless severe displacement effects prevail the low temperature epitaxy method should work and provide an effective means of activating ion implanted impurities in sensitive materials.